ABSTRACT

[0080] A method of fabricating an interconnect structure (e.g., dual damascene interconnect structure, and the like) of an integrated circuit device is disclosed. The interconnect structure is fabricated using a bi-layer mask comprising an imaging film and an organic planarizing film. The bi-layer mask is used to remove lithographic misalignment between a contact hole, a trench, and an underlying conductive line when the interconnect structure is formed. Additionally, a sacrificial layer may be used to protect an inter-metal dielectric (IMD) layer during subsequent planarization of the interconnect structure. The sacrificial layer may be formed of amorphous silicon (Si), titanium nitride (TiN), tungsten (W), and the like. The interconnect structure may be formed of a metal (e.g., copper (Cu), aluminum (Al), tantalum (Ti), tungsten (W), titanium (Ti), and the like) or a conductive compound (e.g., tantalum nitride (TaN), titanium nitride (TiN), tungsten nitride (WN), and the like).